

## T-Kernel for multi-core processors

### Product Overview

The eT-Kernel Multi-Core Edition (eTK MCE) is a real time operating system for next-generation embedded systems with multi-core. It is ideal for high performance embedded systems such as digital home appliances, in-car navigation and entertainment systems, and mobile devices. This RTOS is loaded with features specific to multi-core software development, making the technology accessible even for first-time users.

### Key Features

- ❑ Symmetric multiprocessing (SMP)
- ❑ Co-existence of SMP and AMP programs – blended multiprocessing features
- ❑ Supports four blended scheduling modes to meet various needs of the system
- ❑ Guarantees real time (deterministic) behavior
- ❑ Provides the highest and optimum throughput for the entire system
- ❑ Uses regular APIs for communication and synchronization between programs on different cores
- ❑ Easy software migration from single core to multi-core environments
- ❑ Open-spec kernel API (eT-Kernel)
- ❑ Extensive POSIX support
- ❑ ARM11 MPCore support
- ❑ Drop-in BSP for Renesas Electronics' NaviEngine iPD 35001F5-MN1 (ARM MPCore)

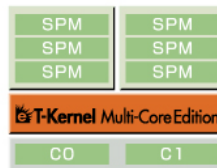
### Scheduling Method

In an eT-Kernel Multi-Core Edition-based system, one or more AMP and SMP programs can coexist on a multi-core processor with a unified eT-Kernel Multi-Core Edition. The system structure is versatile and flexible, with advantages from both AMP and SMP types, depending on the program's intended purpose.

This is achieved by the unique scheduling method of the eT-Kernel Multi-Core Edition. There are four scheduling modes available. Select a mode when generating a task. Priority-based scheduling is applied based on the scheduling mode.

#### SPM Single Processor Mode

Single Processor Mode is a task-scheduling mode that operates a task on the core of a single-core CPU unit. It assures realtime behavior of the system.

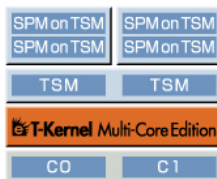


##### Advantages

- Reuse existing software from a single-processor system, that was not originally intended for a multi-core processor
- Guarantees real-time behavior for individual processes just like with a single processor

#### SPM on TSM Single Processor Mode on TSM cores

SPM on TSM is a task-scheduling mode that operates a task on one specific core that belongs to a multicore CPU unit. It allows reusability of the device drivers.

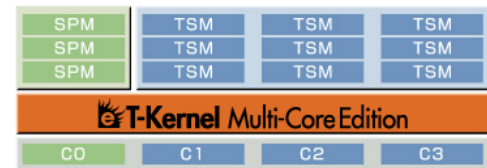


##### Advantages

- Reuse of device drivers
- Achieves both SMP and AMP scheduling in a two-core CPU unit

#### TSM True SMP Mode

True SMP Mode is a task-scheduling mode where the tasks are allocated to the CPU core dynamically, based on the priority of the task. It maximizes the performance of the system.

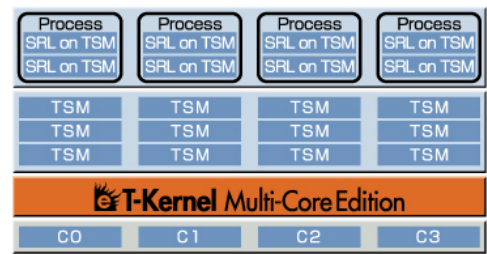


##### Advantages

- Maximizes the performance of an entire system
- Guarantees real-time behavior for individual processes just like with a single processor

#### SRL on TSM Serialize threads on TSM cores

SRL on TSM is a task-scheduling mode that operates a task on any given core that belongs to the multicore CPU unit. It allows SMP scheduling at the scope of the process.



##### Advantages

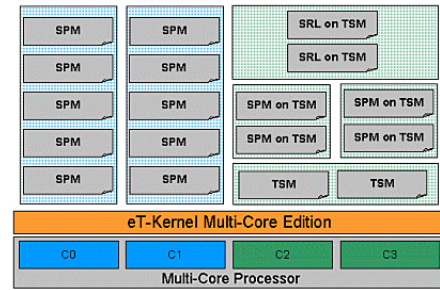
- Allows SMP scheduling at the scope of process
- SMP scheduling can be used for legacy software designed for single-core systems

### Scheduling mode comparisons

Scheduling Mode	Executed Core	Thread migration	Load balance	Interference from other cores
<b>Single Processor Mode (SPM)</b>	SPM Core	No	Fixed upon thread creation	None or minimal
<b>True SMP Mode (TSM)</b>	TSM Core	Yes	Auto balancing by OS	Yes
<b>Single Processor Mode on True SMP (SPM on TSM)</b>	TSM Core	No	Fixed upon thread creation	Yes
<b>Serial on True SMP (SRL on TSM)</b>	TSM Core	Yes	Fixed upon thread creation	Yes

## Core-to-scheduling mode relationships

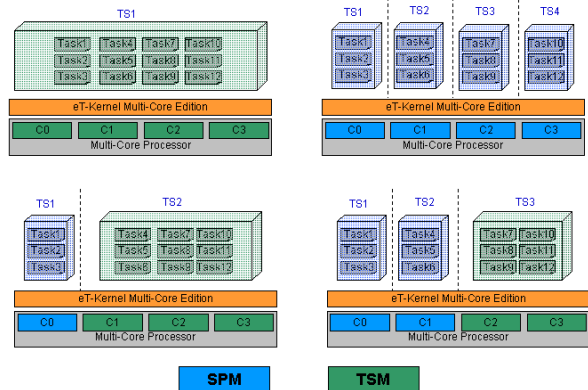
- A SPM core only runs the SPM threads assigned to the core
- A TSM core may run one or more of the following threads in a mixture:
  - TSM threads
  - SPM on TSM thread
  - SRL on TSM threads
- All threads are scheduled based on their priorities, within the bounds of the scheduling mode being used



## Examples of System Configurations

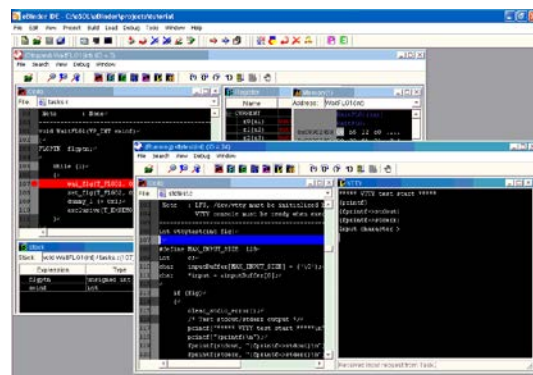
For the ARM11 MPCore multi-core processor, there are up to four different system configurations with mixtures of SMP and AMP, as illustrated in the chart. This is totally user-configurable.

- Task IDs and other OS resources are consistent and unique because a single OS image is used. You can easily use IDs and resources from programs running on different CPU cores.
- You can use the inter-task communication/synchronization services from programs on all CPU cores.
- Preemptive scheduling is based on task priority in both SPM and TSM modes.



## eBinder IDE Solutions for Multi-core Processors

- **Overview:** The eBinder integrated development environment is an embedded system development package that provides a comprehensive range of integrated development tools and software components for debugging multithreaded applications. The eBinder IDE is an Integrated Development Environment with a built-in multicontext debugger for eSOL's real time kernels (PrKERNELv4/eT-Kernel) and is seamlessly integrated with the kernel and middleware products from eSOL (TCP/IP, file system, and USB stack) as an out-of-the-box solution.
- **Package Contents:** eBinder includes a cross compiler, an RTOS-aware multicontext debugger, and development tools for system configuration, system build, advanced testing, and optimization.



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